A Physical Design Tool for Carbon Nanotube Field-Effect Transistor Circuits

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In this article, we present a graphical Computer-Aided Design (CAD) environment for the design, analysis, and layout of Carbon NanoTube (CNT) Field-Effect Transistor (CNFET) circuits. This work is motivated by the fact that such a tool currently does not exist in the public domain for researchers. Our tool has been integrated within Electric a very powerful, yet free CAD system for custom design of Integrated Circuits (ICs). The tool supports CNFET schematic and layout entry, rule checking, and HSpice/VerilogA netlist generation. We provide users with a customizable CNFET technology library with the ability to specify λ-based design rules. We showcase the capabilities of our tool by demonstrating the design of a large CNFET standard cell and components library. Meanwhile, HSPICE simulations also have been presented for cell library characterization. We hope that the availability of this tool will invigorate the CAD community to explore novel ideas in CNFET circuit design.

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1. INTRODUCTION

Given that Complementary Metal-Oxide Semiconductor (CMOS) technology is expected to reach its fundamental scaling limits in the near future, there are tremendous research efforts underway in the material science and device fabrication communities to develop novel nanoscale structures. For possible adoption at the 22-nm technology node, an assortment of multigate devices have been demonstrated including AMD's

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