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Arijit Karmakar · Valentijn De Smedt ·
Paul Leroux

Integrated Time-Based Signal Processing Circuits for Harsh Radiation Environments

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Preface

This research primarily focuses on designing and implementing new architectures for integrated data converters based on time-based signal processing for critical reliability applications in harsh radiation environments. The radiation-hardened integrated circuits (ICs) were developed anticipating high radiation tolerance levels, particularly suited for high-energy physics (HEP) experiments, critical long-term space missions, and future nuclear-operated power plants. Mixed-signal interfaces like sensor readouts (resistive, capacitive, etc.) and clock interfaces are integral parts of various such critical applications, requiring assurance of reliable operation. In the presence of ionizing radiation, total ionizing dose (TID) effects arise due to long-term exposure, gradually changing the threshold voltage, charge carrier mobility, and leakage current of complementary metal-oxide-semiconductor (CMOS) transistors, which affects the performance of analog circuits. Single-event effects (SEEs) are instantaneous disturbances from charge deposition in the silicon (Si) when a charged particle strikes a sensitive node. In typical voltage- or current-based signal processing, the analog-to-digital converters (ADCs) comprise multiple voltage amplifiers, integrators, and comparators, the performance of which is significantly degraded by TID. Although TID effects can be minimized using smaller technology nodes (thin gate oxides), the impact of SEEs increases considerably. Time-based circuits designed in scaled CMOS technologies are relatively robust to TID. Also, in harsh radiation environments, time-based techniques make it easier to counter SEEs by employing various radiation-hardened-by-design (RHBD) techniques (majority voters, functional redundancy, C-element, etc.). The symbiosis between scaled technologies and RHBD techniques works to the advantage of time-based signal processing over voltage-domain signal processing.

As a part of this research, three CMOS-based IC prototypes were implemented in a commercial 65 nm CMOS technology and tested for performance validation and proposed working principles. Two different types of quadrature LC oscillators were implemented in the first project. The sensitivity of different performance parameters of the working prototypes with respect to TID was studied using X-ray irradiation (TID $\leq$100 Mrad (SiO_2)). Next, a radiation-hardened time-based $\Delta\Sigma$ capacitance-to-digital converter (CDC) was

implemented based on MASH 1-0 configuration. The prototypes were validated experimentally in a radiation-less lab environment and with heavy-ion exposure (Xe-ion with LET 65 MeV.cm^2/mg). The CDCs could measure capacitance in the range of 0–3.75 pF with a clock of 100 MHz and have achieved ENOB of 12.9 bits with an energy efficiency of 0.18 pJ/conversion-step. Finally, in the third project, a differential $\Delta\Sigma$ time-to-digital converter (TDC) was implemented with a maximum T_{range} of 98(=±49) ns. It uses a time-based FIR filter in feedback to configure the first, second, and third orders of $\Delta\Sigma$-modulation. It consumes 11–15.8 μW from a 0.6 V supply and achieves the best state-of-the-art energy efficiency in the range of 15.6–89.2 fJ/conversion-step at 10 MHz clock frequency across multiple orders ($\leq$3) of $\Delta\Sigma$-modulation.

In addition, the research findings were valorized by collaborating with an industrial partner to develop a radiation-hardened frequency synthesizer for future space missions. During the research exploitation, several radiation-hardened on-chip integrated circuit components (a digitally-controlled oscillator, a multi-modulus divider, and output buffers) of an all-digital-phase-locked-loop (ADPLL) were implemented and characterized under ionizing radiation.

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